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Numerical study on off-current features in an organic transistor by controlling electrode-overlap area

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ABSTRACT

We investigate the effect of the source/drain-to-gate electrode overlap area on the off-current features in organic thin-film transistors (OTFTs). For the numerical simulation, we used 2-D Atlas, a device simulator based on a two-dimensional Technology Computer Aided Design (TCAD) software tool provided by Silvaco. Both channel and overlap lengths are varied from 1 μm to 1000 μm. The off-current decreases with increasing channel length, whereas variations in the overlap area show a negligible effect on both on- and off-state currents.

KEYWORDS

Numerical Study; Off-state features; Thin-film transistor; Electrode overlap

Introduction

Organic thin-film transistors (OTFTs) are one of the representative device types in the field of organic electronics and have attracted considerable attention due to their outstanding potential in various applications such as active matrix displays, sensors, smart cards, and radio frequency tags [1–4]. Many attempts to improve their performance have therefore been made during the last few decades. As a result of such an enormous amount of research effort, the on-state performance characteristics of these devices (e.g., mobility) have been sufficiently improved. However, because of the ever-increasing need for scaling down and increased integration levels, the off-state features have become increasingly important, and are now as crucial as the on-state characteristics [5]. As a result, the study of off-state properties is in the current research agenda. Some of this research work has recently discussed the effect of electrode overlap in the electrical characteristics of transistors with nanowire structures [6]. Similar studies have also been made for transistors based on vacuum processes, but the electrode overlap effect on transistors with other materials and structures, such as solution-processed flexible OTFTs, has not yet been studied in detail.

In this study, we systematically describe the effect of electrode overlap on OTFT performance through numerical simulations and investigate the relation between the electrode overlap effect and the off-current features at zero-frequency operation. The electrical characteristics were evaluated in a feasible range of both channel and electrode overlap lengths. We also

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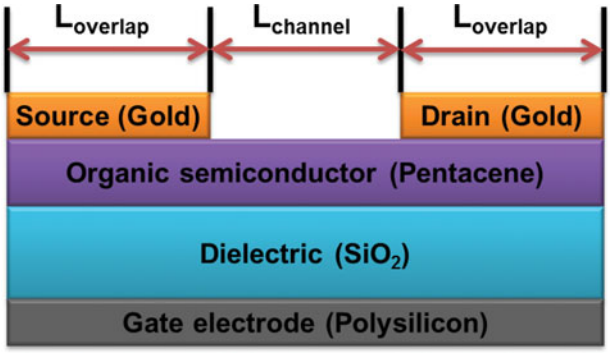

Figure 1. Schematic illustration of the simulated OTFT. Channel and source/drain to gate overlap lengths is varied 1 μm, 10 μm, 100 μm, and 1000 μm, respectively.

suggest some topics for further studies concerning the off-current features and the frequency behavior of OTFTs.

Simulation methodology

Figure 1 illustrates the structure of an OTFT device with a top-contact structure; the channel length is $L_{channel}$, and the source/drain-to-gate electrode overlap length is represented by $L_{overlap}$. The gate electrode and dielectric are made of p-doped polysilicon and SiO_2, respectively; the gate dielectric is 100-nm thick. The source/drain electrodes are made of 10-nm thick gold thin film, with a work function of 5.1 eV. The properties assumed for the active layer are based on pentacene, which is a small molecule classic material that acts as a p-type organic semiconductor; its parameters are taken from [7–9]. In this study, the active layer was considered to be a p-doped semiconductor with a 1×16 cm^{-3} concentration; its detailed parameters are described in Table 1.

For the numerical simulation, we used Atlas, a two-dimensional Technology Computer Aided Design (TCAD) device simulator from Silvaco [10]. With Atlas, we can estimate the electrical characteristics of the device operation for a particular physical structure and bias condition, solving the Poisson and continuity partial differential equations, given in Equations (1) and (2) for the case of hole based conductivity:

$$\varepsilon \nabla^2 \psi = -pq \tag{1}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} \nabla \cdot J_p + G_p - R_p \tag{2}$$

Table 1. Simulation parameters for each material.

Region	Gate Dielectric	Source / Drain	Organic Semiconductor			
Material	SiO2	Gold	Pentacene			
Parameter	Relative permittivity	Work-function	Relative permittivity	Bandgap	Electron affinity	Effective Density of State of conduction (Nc) / valence band (Nv)
Value	3.9	5.1 eV	3.9	2.2 eV	2.8 eV	$2{\cdot}10^{21}$ cm^{-3}

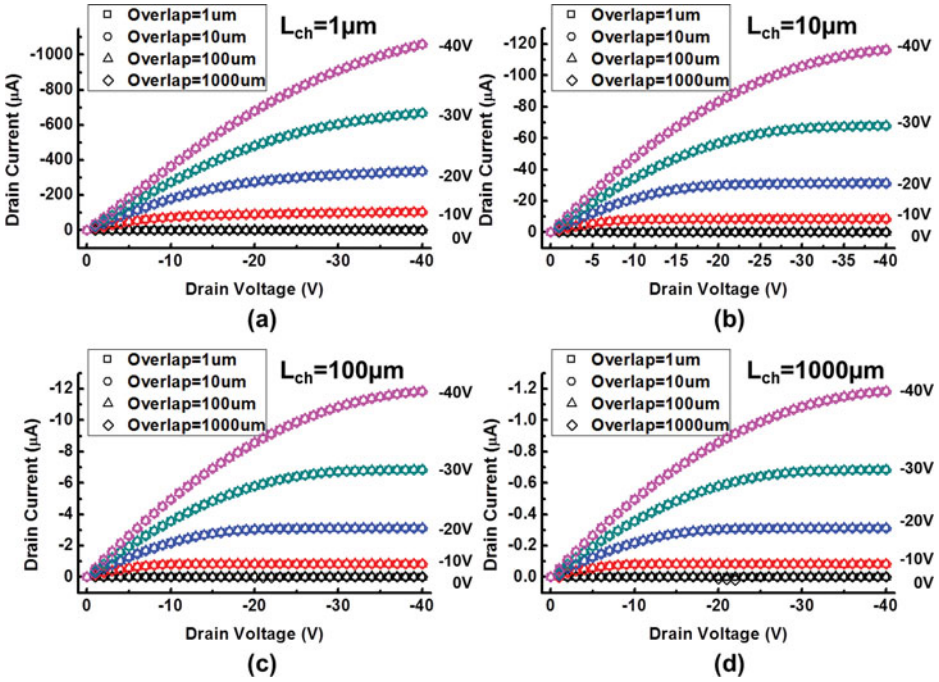

Figure 2. Output characteristics (drain current versus drain voltage) of the simulated OTFT for various electrode overlap lengths; forward sweep of drain voltage (off to on) from 0 V to −40 V, at −10 V step increments of gate voltage from 0 V to −40 V. (a) 1 μm, (b) 10 μm, (c) 100 μm, and (d) 1000 μm channel length.

where ε is the relative permittivity, Ψ is the potential, p is the local hole density, q is the fundamental electronic charge, G_p is the charge generation rate, R_p is the charge recombination rate, and J_p is the current density. The current density, which depends on the drift and diffusion parameters, is given by Equation (3):

$$J_p = qp\mu_p F + qD_p \nabla p \tag{3}$$

where μ_p is the hole mobility, F is the electric field, and D_p is the hole diffusion coefficient.

Results and discussion

Figure 2 shows the output characteristics of the simulated OTFT for various channel and overlap lengths. Figures 2(a), 2(b), 2(c), and 2(d) are regarded as channel lengths of 1 μm, 10 μm, 100 μm, and 1000 μm, respectively. The same length values were considered for the electrode overlap, in each one of those cases. The output characteristics were measured in the forward sweep of drain voltage (off to on) from 0 V to −40 V, at −10 V step increments of gate voltage from 0 V to −40 V. The maximum absolute values of the drain current were 1059.1 μA, 116.3 μA, 11.8 μA, and 1.2 μA, for channel lengths of 1 μm, 10 μm, 100 μm, and 1000 μm, respectively, at −40 V of drain and gate voltages. These figures show a clear pinch-off and an ideal saturation behavior. From the MOSFET equation, the saturation drain current is inversely proportional to the channel length; the results therefore show good agreement with the theory. As can be seen, changing the electrode overlap area does not change the current values. This indicates that the on-state current is not affected by the electrode overlap; this can be explained by the distribution of electric field. When the carriers are injected from the thin-film electrode, they are injected almost from the edge of the electrode close to the channel

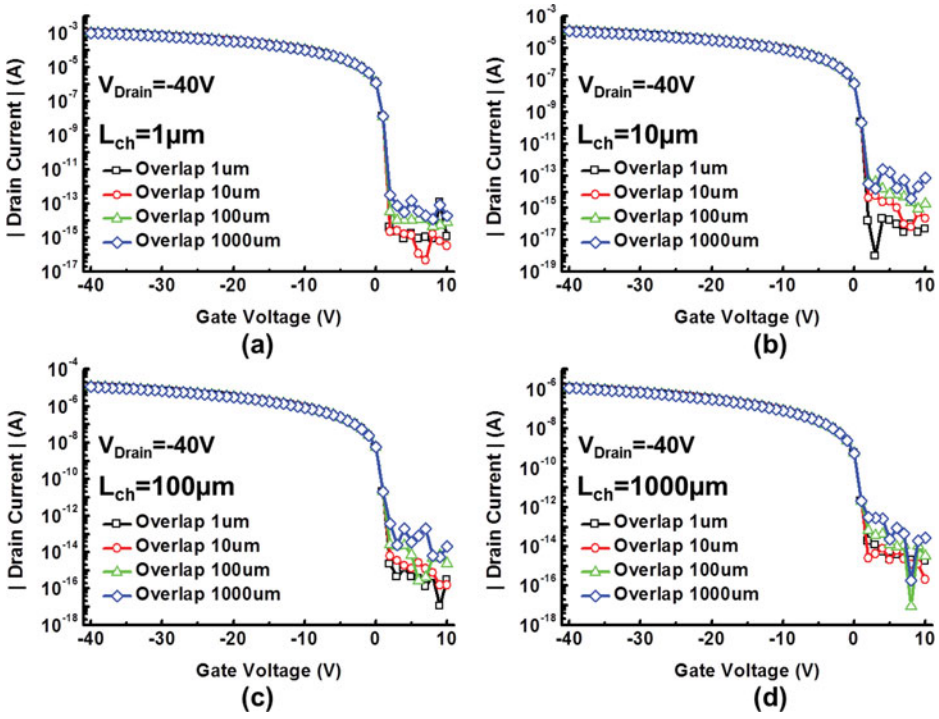

Figure 3. Transfer characteristics (log plot of absolute drain current versus gate voltage) of the simulated OTFT for various electrode overlap lengths; forward sweep of gate voltage (off to on) from 10 V to −40 V in −1 V increments with −40 V of drain voltage. (a) 1 μm, (b) 10 μm, (c) 100 μm, and (d) 1000 μm channel length.

because that is where the electric field is the strongest [11]. This electric field is strong enough to reduce the contact barrier and carriers are therefore injected from this part of electrode.

Figure 3 shows the transfer characteristics of the simulated OTFT for various channel and overlap lengths. As before, both the electrode overlap and channel length vary from 1 μm to 1000 μm. The transfer characteristics were obtained at a fixed drain voltage of −40 V, and the gate voltage was swept from 10 V to −40 V in −1 V increments. The on-state currents (in the 0 V to −40 V gate voltage range, approximately) did not noticeably differ between each other; the off-state currents (in the 10 V to 2 V of gate voltage), however, changed with varying overlap area, with the average current level increasing as the electrode overlap length increased. In this case, a changing bias may produce a different electric field distribution and, consequently, different carrier movements; this may affect the precision of the analysis. We therefore chose only one point, the zero-bias point with Vg - Vth = 0 V. At this threshold gate bias, the transistor is theoretically in the off-state condition.

Figure 4 shows the off-current behavior as a function of the channel length for various overlap lengths, at an effective gate voltage of 0 V. The obtained off-state current values were extracted at $V_g - V_{th} = 0$ V and each value are as follows: 1.28 μA for 1 μm, 60.32 nA for 10 μm, 5.71 nA for 100 μm and 0.57 nA for 1000 μm channel length, respectively. From MOSFET theory, the drain current is inversely proportional to the channel length. This result means that the electrode overlap area does not affect the current features in thin-film structured transistors, where currents are only injected from the edge of the electrode in which the electric field is strongest [11].

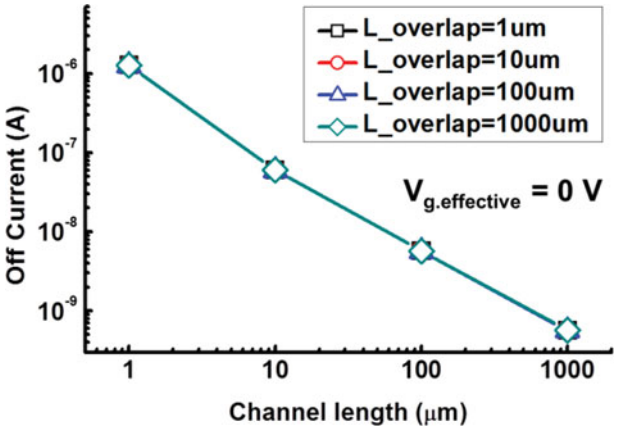

Figure 4. Off-current versus channel length for different electrode overlap lengths, at an effective gate voltage of 0 V.

Figure 5(a) represents the conduction current density distribution in the simulated OTFT for $L_{channel} = L_{overlap} = 10\ \mu m$, at the saturation bias point ($V_{drain} = V_{gate} = -40$ V). The scale is color coded in the legend: black for 10^0 A/cm^2, grey for $10^{1.7}$ A/cm^2, and white for $10^{3.5}$ A/cm^2, respectively. This figure clearly shows that the current is injected at the edge of the

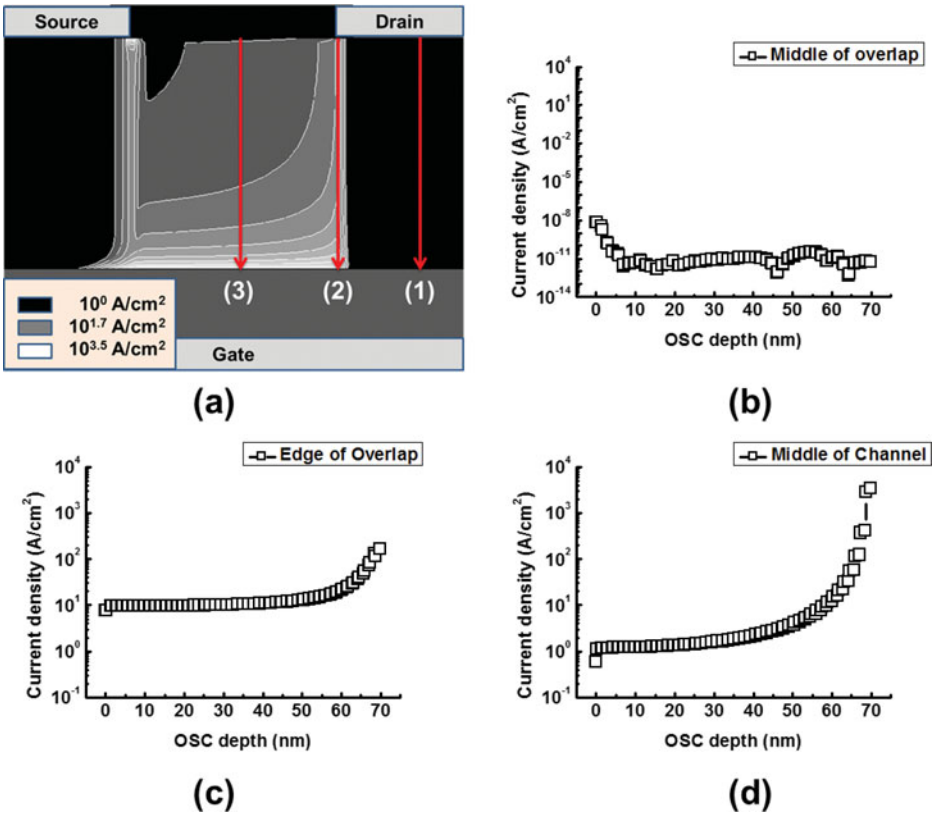

Figure 5. (a) Current density distribution in organic semiconductor (OSC), for $L_{channel} = L_{overlap} = 10\ \mu m$, $V_{drain} = V_{gate} = -40$ V; color coded density values. (b) Current density versus OSC depth at cut line (1). (c) Current density versus OSC depth at cut line (2). (d) Current density versus OSC depth at cut line (3).

electrode and moves vertically to the channel; after passing through the channel, it enters the other electrode edge, in a process identical to the one verified in the injection. For a more specific analysis, we took cross sections of the organic semiconductor (OSC) at three different cut lines: cut line (1) is completely within the electrode overlap, cut line (2) is at the edge of the electrode region, and cut line (3) is in the middle of channel, as shown in Figure 5(a). The cut lines start to the interface between the source/drain electrode and the OSC (0 nm) and end at the interface between the OSC and the gate dielectric (70 nm). Figure 5(b) shows the data for cut line (1); as can be seen, the current density is very small in this region, small enough to be disregarded. At the edge of the overlap (cut line (2), in Figure 5(c)), the current density exhibits much higher levels than the average levels of figure 5(b). Because of the channel, the current density in the 60–70 nm range (induced channel thickness) shows higher values than at OSC depths under 60 nm. We can see this more clearly in Figure 5(d), which corresponds to the middle channel cut line (3); in this case, the current densities at OSC depths above 60 nm present much higher values than the ones in Figure 5(c), while the current densities below the 60 nm depth behave in exactly the opposite way, presenting lower values than the ones in Figure 5(c).

Conclusion

We investigated the off-current features of OTFTs with varying channel and electrode overlap lengths, based on numerical device simulation. Variations in the electrode overlap area do not affect the on- and off-state current features; variations in the channel length, on the other hand, affect the off-current at zero-frequency operation. However, the characteristics of the OTFTs with various frequency will be distinct from the ones at zero-frequency, and remain open to further research. We hope that this study can help device designers understand the independency between the electrode overlap area and the current features in OTFTs at zero-frequency.

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